Amendments to the Drawings

Applicants submit a replacement sheet for the drawing corresponding to Figure 1.

REMARKS

Summary of Office Action

Claims 4-8 are pending. These claims have been rejected under 35 U.S.C. § 112, first and second paragraphs, and under 35 U.S.C. § 102(b) as being anticipated by Cmelik et al. U.S. Patent No. 6,031,992 ("Cmelik"). Further, the drawing has been objected to.

Applicants' Reply

Applicants submit a replacement sheet (informal) for FIG. 1. Applicants will submit a formal drawing shortly.

Applicants have amended the claims to remove the negative limitation to overcome the § 112 rejection. Applicants respectfully traverse the prior art rejection.

As previously noted, claims 4 and 7 specifically recite that the operation of the processor is divided in two parts (1) an execution phase, and (2) a preceding configuration phase. According to applicant's invention, the program code translation is fully completed in the preceding configuration phase (e.g., in a compiler) so that the fully translated instruction words can be used directly in the subsequent execution phase (without, for example, any need for recourse to a translation buffer between the execution phase and the configuration phase).

Cmelik does not show, teach or suggest at least this feature of applicants' invention. Cmelik, as previously noted, is directed to translating program code commands during or congruently with execution of the commands. Cmelik describes a procedure for translation according to conditional branches during program execution. See col. 19, ln. 31 – col. 20, ln. 4.

This is in contrast to applicants' unconditional translation, which occurs not contemporaneously with execution but beforehand.

Here, applicants further note that Cmelik (see e.g., Fig. 2 and Fig. 7, and col. 15, lines 40- col. 16 line 13) uses a translation buffer for storing the translation of a target instruction to be executed by the processor. If a target instruction occurs later, which has the same translation as that already stored in the translation buffer that translation is recalled and a second translation is avoided. Other wise, the second translation must be carried out.

Applicants here also note that Cmelik et al. does not relate to "complex words" which are required by applicants' claims. As described in the specification ¶ [0005], in the prior art execution of a data-stationary command various steps are carried out in several beats. "Each of these steps is carried out by an instruction word part in one instruction word of a sequence of instruction words, each instruction word part prompting a functional unit of the processor to perform a certain action carrying out a partial step of the execution of the command.

Each instruction word, according to the known approach, must be newly composed over the sequence of program words. Even in the case of performing identical commands, it is necessary to generate instruction words corresponding to the partial steps of each command and to compose the program words for this purpose. This is necessary also in the case of identical commands, that is, for like command sequences, new, albeit identical program word sequences are required again and again. This entails a large memory utilization and considerable processing time."

In applicants' invention, a data stationary command is related to various instruction word parts in a secondary instruction word 15 (stored in the secondary instruction word memory 7). Each of these steps in the execution of the data stationary command is carried out by an instruction word part. (A secondary instruction word of the invention may be similar to a target instruction in Cmelik et al.)

In applicants invention, the secondary instruction word memory 15 is provided with memory capacity for storing multiple secondary instruction words, so that the instruction word parts belonging to a data-stationary command can be transferred (i.e. stored or exchanged) into the relating rows and columns of the instruction word memory or with other words into the relating places of the sequenced secondary instruction words (VLIW).

This procedure is neither shown nor suggested by Cmelik et al. In particular, the features of the applicants' invention namely (1) "during the preceding configuration phase instruction word parts corresponding to data-stationary commands splitted on several instruction words are assembled as complex words in a complex word sequence," (claim 4) and (2) that the "complex words are read from said complex word table and stored in parallel in the corresponding rows and columns of said secondary instruction word memory" (claims 4 and 7) are not shown or suggested by Cmelik.

Accordingly, for at least the foregoing reasons claims 4 and 7 and their dependent claims 5, 6 and 8 are patentable over Cmelik et al.

Conclusion

This application is now in condition for allowance. Reconsideration and prompt allowance of which are requested. If there are any remaining issues to be resolved, applicants request the Examiner to kindly contact the undersigned attorney by telephone.

Respectfully submitted,

BAKER BOTTS L.L.P.

By: _____

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